

WEST Search History

DATE: Monday, December 11, 2006

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| | | <i>DB=PGPB,USPT; THES=ASSIGNEE; PLUR=YES; OP=ADJ</i> | |
| <input type="checkbox"/> | L2 | (simulat\$ same target processor) and ((decrease ro reduc\$) same development time) | 0 |
| <input type="checkbox"/> | L1 | maurudis.in. and simulat\$ and target processor? | 3 |

END OF SEARCH HISTORY

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Search Results - Record(s) 1 through 3 of 3 returned.

☐ 1. Document ID: US 20040128119 A1

L1: Entry 1 of 3

File: PGPB

Jul 1, 2004

PGPUB-DOCUMENT-NUMBER: 20040128119

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040128119 A1

TITLE: Method and apparatus for accurately modeling digital signal processors

PUBLICATION-DATE: July 1, 2004

INVENTOR-INFORMATION:

| NAME | CITY | STATE | COUNTRY |
|---------------------------------|------------|-------|---------|
| <u>Maurudis</u> , Anastasios S. | Manchester | CT | US |
| Della Morte, John O. JR. | Forestdale | MA | US |
| Della Morte, James T. | Sandwich | MA | US |

US-CL-CURRENT: 703/14

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KVMC | Draw D |
|------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|--------|------|--------|
|------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|--------|------|--------|

☐ 2. Document ID: US 6741958 B1

L1: Entry 2 of 3

File: USPT

May 25, 2004

US-PAT-NO: 6741958

DOCUMENT-IDENTIFIER: US 6741958 B1

TITLE: Method and apparatus for accurately modeling digital signal processors

DATE-ISSUED: May 25, 2004

INVENTOR-INFORMATION:

| NAME | CITY | STATE | ZIP CODE | COUNTRY |
|---------------------------------|------------|-------|----------|---------|
| <u>Maurudis</u> , Anastasios S. | Manchester | CT | 06040 | |
| Della Morte, Jr.; John O. | Forestdale | MA | 02644 | |
| Della Morte; James T. | Sandwich | MA | 02563 | |

US-CL-CURRENT: 703/27; 703/20, 703/23

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Patents | Abstracts | Claims | KWC | Draw. De |
|------|-------|----------|-------|--------|----------------|------|-----------|---------|-----------|--------|-----|----------|
|------|-------|----------|-------|--------|----------------|------|-----------|---------|-----------|--------|-----|----------|

☐ 3. Document ID: US 6173247 B1

L1: Entry 3 of 3

File: USPT

Jan 9, 2001

US-PAT-NO: 6173247

DOCUMENT-IDENTIFIER: US 6173247 B1

TITLE: Method and apparatus for accurately modeling digital signal processors

DATE-ISSUED: January 9, 2001

INVENTOR-INFORMATION:

| NAME | CITY | STATE | ZIP CODE | COUNTRY |
|---------------------------|------------|-------|----------|---------|
| Maurudis; Anastasios S. | Manchester | CT | | |
| Della Morte, Jr.; John O. | Forestdale | MA | | |
| Della Morte; James T. | Sandwich | MA | | |

US-CL-CURRENT: 703/23; 703/20, 703/22, 703/27

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Patents | Abstracts | Claims | KWC | Draw. De |
|------|-------|----------|-------|--------|----------------|------|-----------|---------|-----------|--------|-----|----------|
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|-------|---------------------|-------|----------|-----------|---------------|
| Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS |
|-------|---------------------|-------|----------|-----------|---------------|

| Term | Documents |
|--|-----------|
| MAURUDIS | 5 |
| MAURUDI | 0 |
| TARGET | 547863 |
| TARGETS | 132319 |
| SIMULAT\$ | 0 |
| SIMULAT | 2 |
| SIMULATABLE | 18 |
| SIMULATANEOUS | 12 |
| SIMULATANEOUSLY | 26 |
| SIMULATE | 5878 |
| SIMULATED | 6909 |
| (MAURUDIS.IN. AND SIMULAT\$ AND TARGET PROCESSOR?).PGPB,USPT. | 3 |

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DATE: Monday, December 11, 2006

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|--------------------------|---------------------------|---|----------------------------|
| | | <i>DB=PGPB,USPT; THES=ASSIGNEE; PLUR=YES; OP=ADJ</i> | |
| <input type="checkbox"/> | L4 | (382/243.ccls or 717/104,135.ccls. or 708/495.ccls) and (simulat\$ same target processor) and ((decrease or reduc\$) same development time) | 1 |
| <input type="checkbox"/> | L3 | 382/243.ccls and 717/104,135.ccls. and 708/495.ccls and (simulat\$ same target processor) and ((decrease or reduc\$) same development time) | 0 |
| <input type="checkbox"/> | L2 | L1 and (simulat\$ same target processor) and ((decrease or reduc\$) same development time) | 3 |
| <input type="checkbox"/> | L1 | 703/2,13,20,23,26,27.ccls. | 4225 |

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Search Results - Record(s) 1 through 3 of 3 returned.

☐ 1. Document ID: US 20020059054 A1

L2: Entry 1 of 3

File: PGPB

May 16, 2002

PGPUB-DOCUMENT-NUMBER: 20020059054

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020059054 A1

TITLE: Method and system for virtual prototyping

PUBLICATION-DATE: May 16, 2002

INVENTOR-INFORMATION:

| NAME | CITY | STATE | COUNTRY |
|------------------------|------------|-------|---------|
| Bade, Stephen L. | Lindon | UT | US |
| Ben-Chorin, Shay | Cupertino | CA | US |
| Caamano, Paul | San Mateo | CA | US |
| Montoreano, Marcelo E. | Santa Cruz | CA | US |
| Taggu, Ani | Campbell | CA | US |
| Thoen, Filip C. | San Jose | CA | US |
| Wills, Dean C. | Corvallis | OR | US |

US-CL-CURRENT: 703/20

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Drawings |
|------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|--------|------|----------|
|------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|--------|------|----------|

☐ 2. Document ID: US 6741958 B1

L2: Entry 2 of 3

File: USPT

May 25, 2004

US-PAT-NO: 6741958

DOCUMENT-IDENTIFIER: US 6741958 B1

TITLE: Method and apparatus for accurately modeling digital signal processors

DATE-ISSUED: May 25, 2004

INVENTOR-INFORMATION:

| NAME | CITY | STATE | ZIP CODE | COUNTRY |
|---------------------------|------------|-------|----------|---------|
| Maurudis, Anastasios S. | Manchester | CT | 06040 | |
| Della Morte, Jr.; John O. | Forestdale | MA | 02644 | |

Della Morte; James T.

Sandwich

MA

02563

US-CL-CURRENT: 703/27; 703/20, 703/23

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Excluded | Amendments | Claims | KAMC | Draw De |
|------|-------|----------|-------|--------|----------------|------|-----------|----------|------------|--------|------|---------|
|------|-------|----------|-------|--------|----------------|------|-----------|----------|------------|--------|------|---------|

☐ 3. Document ID: US 6173247 B1

L2: Entry 3 of 3

File: USPT

Jan 9, 2001

US-PAT-NO: 6173247

DOCUMENT-IDENTIFIER: US 6173247 B1

TITLE: Method and apparatus for accurately modeling digital signal processors

DATE-ISSUED: January 9, 2001

INVENTOR-INFORMATION:

| NAME | CITY | STATE | ZIP CODE | COUNTRY |
|---------------------------|------------|-------|----------|---------|
| Maurudis; Anastasios S. | Manchester | CT | | |
| Della Morte, Jr.; John O. | Forestdale | MA | | |
| Della Morte; James T. | Sandwich | MA | | |

US-CL-CURRENT: 703/23; 703/20, 703/22, 703/27

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Excluded | Amendments | Claims | KAMC | Draw De |
|------|-------|----------|-------|--------|----------------|------|-----------|----------|------------|--------|------|---------|
|------|-------|----------|-------|--------|----------------|------|-----------|----------|------------|--------|------|---------|

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| Term | Documents |
|--|-----------|
| TARGET | 547863 |
| TARGETS | 132319 |
| PROCESSOR | 559605 |
| PROCESSORS | 186862 |
| DECREASE | 833972 |
| DECREASES | 631987 |
| DEVELOPMENT | 782958 |
| DEVELOPMENTS | 84818 |
| TIME | 3523597 |
| TIMES | 1762083 |
| SIMULAT\$ | 0 |
| (L1 AND (SIMULAT\$ SAME TARGET PROCESSOR) AND ((DECREASE OR REDUC\$) SAME DEVELOPMENT TIME)).PGPB,USPT. | 3 |

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Search Results - Record(s) 1 through 1 of 1 returned.

☐ 1. Document ID: US 6741958 B1

L4: Entry 1 of 1

File: USPT

May 25, 2004

US-PAT-NO: 6741958

DOCUMENT-IDENTIFIER: US 6741958 B1

TITLE: Method and apparatus for accurately modeling digital signal processors

DATE-ISSUED: May 25, 2004

INVENTOR-INFORMATION:

| NAME | CITY | STATE | ZIP CODE | COUNTRY |
|---------------------------|------------|-------|----------|---------|
| Maurudis; Anastasios S. | Manchester | CT | 06040 | |
| Della Morte, Jr.; John O. | Forestdale | MA | 02644 | |
| Della Morte; James T. | Sandwich | MA | 02563 | |

US-CL-CURRENT: 703/27; 703/20, 703/23

| | | | | | | | | | | | |
|------|-------|----------|-------|--------|----------------|------|-----------|----------|--------|-----|---------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Abstract | Claims | KMC | Draw De |
|------|-------|----------|-------|--------|----------------|------|-----------|----------|--------|-----|---------|

Clear

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Print

Fwd Refs

Bkwd Refs

Generate OACS

| Term | Documents |
|--|-----------|
| 382/243.CCLS | 0 |
| 382/243.CCL | 0 |
| 717/104 | 721 |
| 717/104S | 0 |
| 717/135 | 142 |
| 717/135S | 0 |
| 708/495.CCLS | 0 |
| 708/495.CCL | 0 |
| TARGET | 547863 |
| TARGETS | 132319 |
| PROCESSOR | 559605 |
| ((382/243.CCLS OR 717/104,135.CCLS. OR | |

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| IEEE CNF | IEEE Conference Proceeding |
| IEE CNF | IEE Conference Proceeding |
| IEEE STD | IEEE Standard |

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